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Investigation of a New Topology for Multilevel Inverters Fed by Photovoltaic System for Linear Induction Motor

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Abstract

In this paper, a new structure of multilevel inverters with the reducing the count of utilized power equipment is presented. This inverter consists of two parts, a basic module, and an H-bridge. Since the basic module part is only able to generate positive and zero voltage levels, so the H-bridge is connected to the basic module to generate all levels symmetrically (positive and negative). The newly suggested inverter is investigated by two input source determination algorithms and the general configuration of the converter is proposed with the ability to extend to a high number of levels. From the general structure of the proposed multilevel inverter, one circuit is selected to perform all the simulations, implementations, and other studies on it. Moreover, in order to investigate the proper operation of the proposed structure, this inverter has been simulated in the application of a linear induction motor in which the inverter voltage sources are powered by photovoltaic systems. The power losses of the case-study circuit with symmetrically determined input sources using the NLC modulation method are investigated for three various loads. Besides, to demonstrate the merits and features of the new inverter, the suggested inverter is compared with some recent inverters. Finally, to demonstrate the possibility and function of the suggested multilevel inverter, the case-study circuit is simulated and implemented in MATLAB/Simulink software and power electronics laboratory, respectively.

Keywords: Basic Module; Symmetric Multilevel Inverter; Asymmetric Multilevel Inverter; Cascaded Multilevel Inverter

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Introduction

Recently, multilevel inverters (MLIs) have been widely considered by researchers and are among the most widely used power electronic converters. Since MLIs provide high-quality output voltage and current in converting DC voltage sources to AC, they have gained wide application in the industry. Providing high-quality output waveforms (current and voltage) on the AC side, having fewer problems related to electromagnetic compatibility (EMC), proper division of the task of generating output voltage between inverter switches, proper operation in high voltage/power applications, and less stress on power switches of the inverter are among the most essential advantages of MLIs compared to two-level inverters. Due to the mentioned features in MLIs, these power electronic converters have found wide application in various fields of power electronics. Among the most essential applications of MLIs are active power filters, uninterruptible power supply (UPS), renewable energy conversion, hybrid and electrical vehicles, flexible AC transmission systems (FACTS),

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and high voltage DC (HVDC) [1]. The most famous and industrial classic MLIs are introduced and analyzed as follows.

The first classic MLI is the cascaded H-bridge (CHB), in which to increment the count of voltage levels, the H-bridge units are cascaded together. Since these MLIs have simplicity and the highest modularity compared to other MLIs, they have high reliability. However, the exploitation of isolated input sources for each of the H-bridge units, and increment of the utilized power components in the inverter by increasing the voltage levels is the challenge for these MLIs [2]. Neural point clamped (NPC) is another class of classic MLIs. One of the NPC challenges is the imbalance of voltage of capacitors due to the discharge of the middle capacitors, in which the capacitors' voltage must be controlled. The design of a control algorithm for balancing the capacitors' voltage to prevent neutral point deviation from zero voltage, leads to an increase in inverter complexity and increments the overall cost of the inverter. The third category of MLIs is the flying capacitor (FC). In FC, there are many DC capacitors, which help the inverter to pass through short-term deep flashes, or short-term voltage outages. In FC, the voltage of the capacitors must also be controlled, which increments the complexity and the total expense of the inverter. Therefore, FC like NPC isn't usually used for a high count of levels [3]. Due to the mentioned limitations and challenges in classic MLIs, new structures for MLIs have recently been proposed, some of which are being studied.

One of the recent structures for MLIs is [4]. The presence of only one DC-link has given this structure the ability to be adequately exploited in back-to-back applications. In this work, the LS-PWM is utilized for the inverter switching due to provide appropriate power quality. Due to the exploit of capacitors in this converter, the capacitors' voltage must be controlled to the desired value. Besides, an MLI can boost the voltage as proposed in [5]. In this paper, an attempt is made to decrease the voltage stress on the inverter power components. One of the features of this structure is the self-balancing voltage of the capacitors, which eliminates the necessity for any other circuit to balance the voltage of the capacitors. The power losses of this converter are calculated, and since the efficiency of this topology is 91.7%, in terms of efficiency, this converter is satisfactory. A high count of semiconductors is one of the challenges of this topology. A new 11-level structure called K-type is proposed in [6]. For validation, the introduced converter is simulated and implemented in MATLAB/Simulink and power electronics laboratory, respectively. This structure attempts to reduce the devices in the inverter. However, this proposed topology still suffers from a high count of switches. Another recent MLI is [7]. This structure can boost the voltage, and without any additional circuit, it can produce all levels symmetrically. This structure suffers from a large count of switches and reverses voltage on the switches. A new structure for MLIs, which is step-wise, is proposed in [8]. Since in the proposed topology, generating output voltage is divided between the inverter switches, it is proper for high voltage/power applications. One of the challenges of this structure is a large count of isolated sources. A 15-level inverter is suggested in [9]. In this converter, the low count of switches in the current flow path causes low conduction losses. NLC is used to switch this inverter due to the low switching losses. Despite the efforts made in this paper to reduce inverter components, this structure still suffers from many switches and driver circuits. A new basic circuit for MLIs is recommended in [10]. Since this basic circuit can only generate positive and zero levels, so it is combined with an H-bridge to be able to produce all levels symmetrically. The count of switches and driver circuits in this topology is high, which causes an increase in expense and the total volume of the converter. Another structure that is switch-ladder is proposed in [11]. This structure doesn't use any capacitors, so its control circuit is simple, and its dynamic response speed is great. The NLC fundamental frequency modulation method is utilized in this paper because it has low switching losses and low THD in the inverter voltage. A large count of power equipment in this converter leads to the complexity of the control circuit and increases the volume and total cost of the inverter. Another recent structure for MLIs is [12]. This structure doesn't use any capacitors and has a high dynamic response speed. It should be noted that one of the challenges of this structure is the high number of independent input sources, which is, in practice, the preparation of them is a little complicated.

In this research, a new MLI with the approach to reducing the count of switches and driver circuits is proposed. In section 2, a new basic module (BM) with the capability to generate positive and zero levels is proposed. Since the purpose of this paper is to provide a single-phase MLI, so for the new structure to be able to generate all levels symmetrically, the BM is combined with an H-bridge. In this work, the amplitude of the input sources is determined and studied by two algorithms (symmetric and asymmetric). Moreover, in this section, the utilized maximum power point tracking (MPPT) method is

studied. Also, in section 3, the losses and efficiency of the case-study circuit considering the NLC method are calculated for the symmetric configuration. Moreover, in section 4, to justify the proposed structure, this new inverter is compared with some recently proposed structures for MLIs in viewpoints of the count of power electronic equipment and total standing voltage (TSV) on the switches. Besides, in section 5, Since the new proposed MLI can be used with any number of BMs, in this section, one circuit is considered as a case-study circuit to be done for all the simulations, implementations, and other studies on it. Moreover, in section 5, the two modulation methods of NLC and LS-PWM are used and studied to switch the case-study circuit. In this section to show the feasibility of the proposed structure, the case-study circuit is performed for various modulation indexes and loads by two methods, NLC and LS-PWM, and the THD of its voltage is studied. In this section, the symmetric configuration of the proposed structure for the application of the linear induction motor is simulated and the output waveforms are shown. Finally, to prove the performance of the introduced MLI, in addition to the simulation performed in MATLAB/Simulink, the case-study circuit has been implemented by the NLC and LS-PWM methods in the power electronics laboratory for symmetric configuration.

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2. Proposed Topology and Utilized MPPT

Fig. 1 shows a new BM. As shown in Fig. 1 the suggested BM consists of seven power switches, four voltage sources, and four power diodes. The various BM switching states are provided in Table 1. According to Table 1, there are different switchings, which lead to the production of different voltage levels. Of course, according to Table 1, the proposed BM is only able to produce positive and zero levels. It should be noted that since some switchings, such as simultaneous conduction losses of Sb4 and Sb5, causes a short circuit of some input sources, these

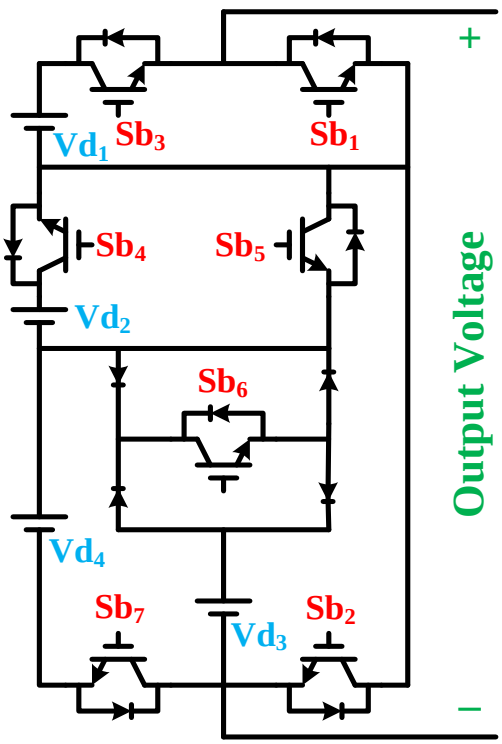


Figure 1. Proposed BM

switchings are not permissible and are not listed in Table 1. Besides, to increment the count of levels and thus decrease the THD of the AC side (current and voltage), as shown in Fig. 2 the BMs are first cascaded together and then connected to an H-bridge to generate whole levels symmetrically. Fig. 2 shows the general configuration of the introduced MLI, and K indicates the number of cascaded BMs. In Table 1, there are two standard voltage source determination algorithms (symmetric and asymmetric), so according to the type of voltage source determination algorithm, two symmetric and asymmetric configurations are named and studied as follows.

Table 1. Available switching states for the BM

State	Sb_1	Sb_2	Sb_3	Sb_4	Sb_5	Sb_6	Sb_7	Output Voltage
1	off	off	on	on	off	off	on	$V_{d1}+V_{d2}+V_{d4}$
2	on	off	off	on	off	off	on	$V_{d2}+V_{d4}$
3	off	off	on	off	on	off	on	$V_{d1}+V_{d4}$
4	on	off	off	off	on	off	on	V_{d4}
5	off	off	on	on	off	on	off	$V_{d1}+V_{d2}+V_{d3}$
6	on	off	off	on	off	on	off	$V_{d2}+V_{d3}$
7	off	off	on	off	on	on	off	$V_{d1}+V_{d3}$
8	on	on	off	off	on	on	off	V_{d3}
9	off	on	on	off	off	off	off	V_{d1}
10	on	on	off	off	off	off	off	0

2.1. First Configuration: Symmetric

In this algorithm, all input sources in the whole MLI are equalized. That is why the structure whose voltage sources are determined by this algorithm is called a symmetric structure. According to Table 1, considering that all input sources are equal, some switching states lead to the same voltage levels. These switching states are known as the redundancy switching states and make the switching algorithm more flexible for various approaches. Moreover, with this algorithm, the structure of the inverter will have the most modularity. As mentioned before, the magnitude of all input sources in this algorithm is equal and is calculated for the proposed topology according to the following equation.

$$V_{1,K}=V_{2,K}=V_{3,k}=V_{4,K}=V_{DC} \quad (1)$$

Also, in the symmetric algorithm, the number of switches (N_s), driver circuits (N_{dr}), isolated input sources (N_{DC}), diodes (N_d), and the number of generated levels on the AC side (N_L) is expressed as follows.

$$N_s=N_{dr}=7K+4 \quad (2)$$

$$N_{DC}=4K \quad (3)$$

$$N_d=4K \quad (4)$$

$$N_L=6K+1 \quad (5)$$

Furthermore, the TSV for the symmetric configuration is given by (6).

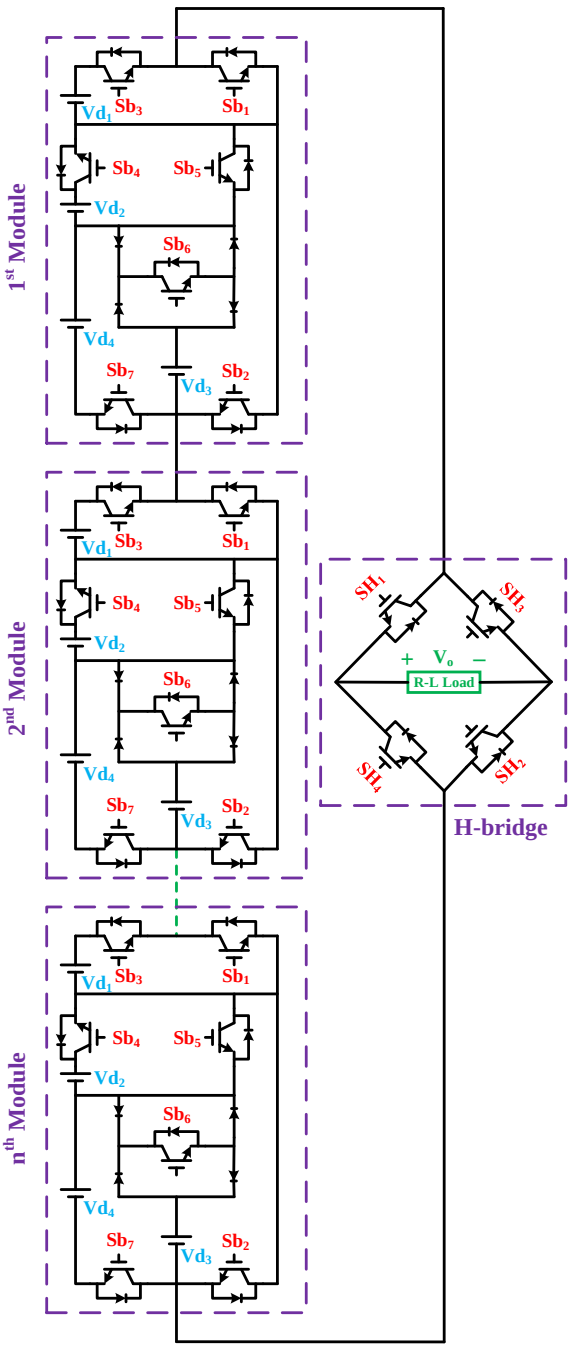


Figure 2. Generic structure of the introduced MLI

$$TSV = 20K \quad (6)$$

2.1. Second Configuration: Asymmetric

In this algorithm, the magnitude of input sources is determined unequally. Since in this algorithm, the amplitude of the input sources is determined asymmetrically, so this structure is named asymmetric structure. In this algorithm, the inverter structure has the highest voltage levels, and there aren't redundancy switching states. Of course, it should be noted that in this algorithm, the modularity of the inverter is largely lost. As mentioned, in this algorithm, the magnitude of input sources is unequal and is determined for the proposed topology as follows.

$$V_{1,K} = 10^{K-1} V_{DC} \quad (7)$$

$$V_{2,K} = V_{3,K} = 2 \times 10^{K-1} V_{DC} \quad (8)$$

$$V_{4,K} = 6 \times 10^{K-1} V_{DC} \quad (9)$$

Furthermore, in the asymmetric configuration, N_s, N_{dr}, N_{DC}, N_d, and N_L are calculated as follows.

$$N_s = N_{dr} = 7K + 4 \quad (10)$$

$$N_{DC} = 4K \quad (11)$$

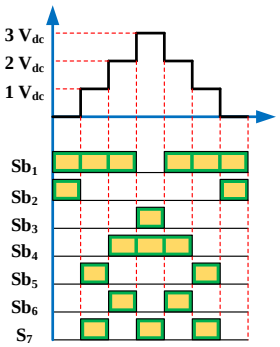
$$N_d = 4K \quad (12)$$

$$N_L = 2 \times 10^K - 1 \quad (13)$$

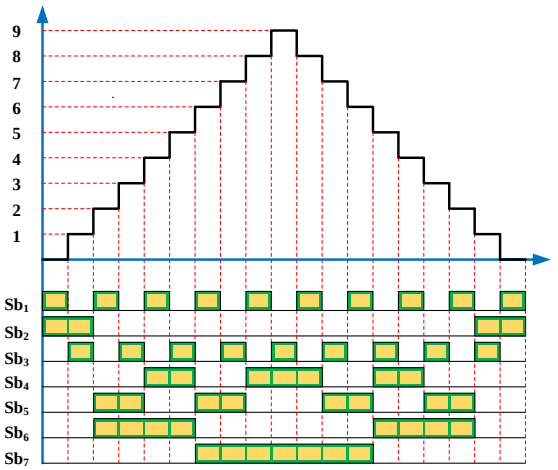
Also, the TSV in the second algorithm is calculated as (14).

$$TSV = \frac{60}{9} \times (10^K - 1) \quad (14)$$

The switching pattern for the generic structure with one BM and H-bridge, which is called a case-study circuit is demonstrated in both symmetric and asymmetric algorithms and shown in Fig. 3(a) and 3(b), respectively.



(a)



(b)

Figure 3. The switching pattern for the case-study circuit in (a) symmetric (b) asymmetric configuration

2.3. Utilized MPPT

There are several methods for MPPT, the classification of which is shown in Fig. 4, each of which has its advantages and disadvantages and can be suitable for different applications. Among the various MPPT methods, the P&O method, which is a traditional method, is intended for simulation due to its simplicity of this MPPT method and the lack of a complex processing system.

In this method, the variable is disturbed and its effect on other variables is observed. Fig. 5 and Fig. 6 show the general concept of the operation of the P&O method, the MPP point of which is tracked by the P&O algorithm. In this method, the load of the module changes until it reaches the MPP so that by measuring the output current and voltage V_1 and adjusting the amount of load, the tracking algorithm is performed. At work point V_1, P_1 is measured and in the next step, the load is increased and at work point V_2, P_2 is measured. Then by comparing P_1 and P_2, since P_2 is greater than P_1, the changes continue in the

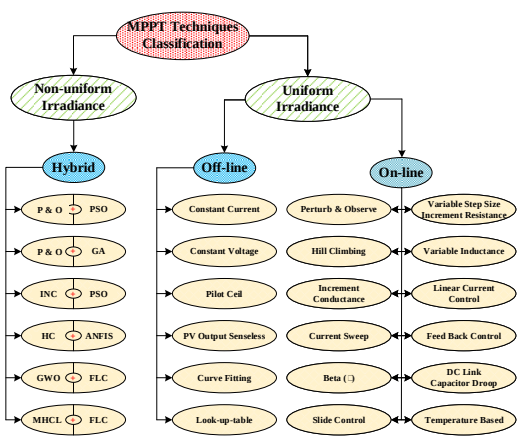


Figure 4. Classification of Various MPPT Methods

same direction. In the next step, the operating point is again switched to voltage V_3 and its power, which is P_3, is measured. As P_3 is larger than P_2, change continues. Then at voltage V_4, P4 is greater than P_3. Finally, since at point V_4, P_5 is smaller than P_4, changes are made in reverse to approach the MPP again, and the P&O algorithm oscillates between P_4 and P_5, which is approximately the MPP. Flowchart

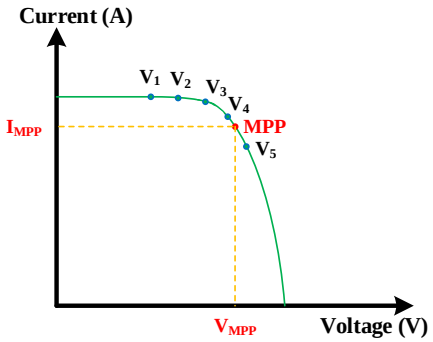


Figure 5. I-V Curve of the PV

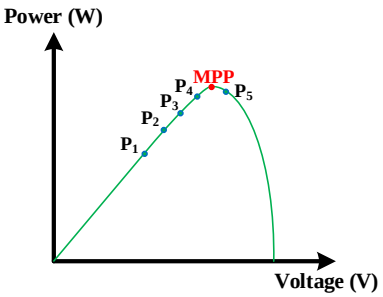


Figure 6. P-V Curve of the PV

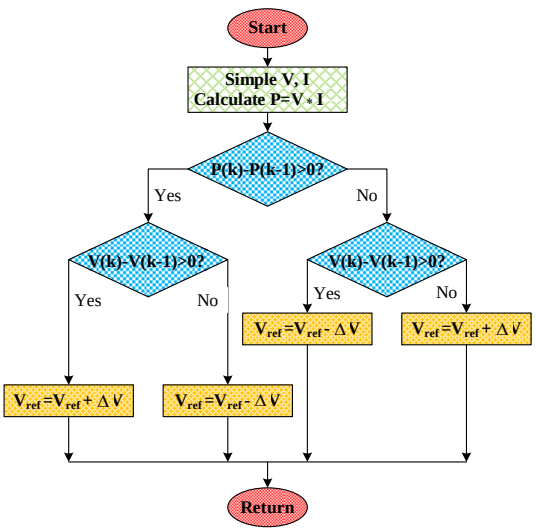


Figure 7. Flowchart of the priciple operation of the P&O

How the P&O method works to track the MPP is shown in Fig. 7 [14].

3. Calculation of Converter Losses and Efficiency

Since the utilized switches in power electronic converters are usually non-ideal, so there are two types of losses, conduction losses, and switching losses. The losses of power electronic converters depend on various parameters such as the type of modulation strategy and the switching frequency of the converter. Therefore, since there are power losses in a power electronic converter, the efficiency of a power electronic converter isn't 100 percent and should be calculated. In this section, first, the conduction and switching losses for the symmetric configuration considering the NLC modulation method for three various loads are calculated, and then the total efficiency of the proposed inverter is calculated [13].

3.1. Conduction Losses

Since in MLIs, many switches and diodes are utilized, so first, the conduction losses for one switch and diode must be calculated, and then the conduction losses for all utilized switches and diodes in the MLI must be obtained. A diode, in the conductive state, can be assumed by a reverse voltage drop of $V_{c,D}$, which is series by a linear and constant resistor of R_D. Therefore, the conduction losses of a diode ($p_{c,D}(t)$) can be expressed as follows.

$$p_{c,D}(t) = \left[V_{c,D} + R_D i(t)\right] i(t) \tag{15}$$

Similarly, a switch in the conduction losses can be modeled as a reverse voltage drop of $V_{c,S}$ with a series linear and constant resistor of R_S. In this case, the losses of the conduction state of a switch ($p_{c,S}(t)$) are obtained by (16).

$$p_{c,S}(t) = \left[V_{c,S} + R_S i^{\beta}(t)\right] i(t) \tag{16}$$

It should be noted that in equation (18), □ is a constant that depends on the characteristics of the utilized switch. Since equation (15), and equation (16) show the instantaneous conduction losses of the diode and switch, so the following equations can be utilized to calculate the average conduction losses of a diode ($P_{c,D}$) and switch ($P_{c,S}$), which are usually are considered for analysis.

$$P_{c,D} = \int_T p_{c,D}(t)dt \tag{17}$$

$$P_{c,S} = \int_T p_{c,S}(t)dt \tag{18}$$

As mentioned before, since there are several switches and diodes in an MLI, the losses of an MLI are the sum of the losses of all utilized switches and

diodes in the converter. So, the total conduction losses (P_c) of an MLI can be calculated as follows.

$$P_c = \sum_{K=1}^{N_D} \frac{1}{\pi} \int_0^{\pi} \left[\left(f_{D,K}(t) V_{D,K} + f_{D,K}(t) R_{D,K} i(t) \right) i(t) \right] d(\omega t) + \sum_{K=1}^{N_S} \frac{1}{\pi} \int_0^{\pi} \left[\left(f_{s,K}(t) V_{s,K} + f_{s,K}(t) R_{s,K} i^{\beta}(t) \right) i(t) \right] d(\omega t) \quad (19)$$

Whereas, K, $f_{D,K}(t)$, and $f_{S,K}(t)$ represent the K^{th} switch or diode, switching function of the diode, and switching function of the switch, respectively. Besides, N_D and N_s represent the count of diodes and the count of switches in the current path, respectively. It should be noted that $f_{D,K}$ is 1 when the diode is in the current path, and $f_{s,K}$ is 1 when the switch is in the current path, otherwise, they will be zero.

According to equation (23), the switching angles in the proposed symmetric configuration considering the NLC modulation method are obtained as follows [13].

$$\alpha_1 = 9.6^{\circ} \quad \alpha_2 = 30^{\circ} \quad \alpha_3 = 56.44^{\circ}$$

By considering the characteristics of the semiconductor in Table 2, the conduction losses for different loads are obtained in Table 3.

Table 2. The characteristics of the utilized semiconductors

Semiconductor	V_{on}	R_{on}	t_{on}	t_{off}
Switch	1.85V	12.13mΩ	258ns	388ns
Diode	2.17V	11.6mΩ	-	-

Table 3. The conduction losses for various loads

Type of Load	Conduction Losses
First Load (R=20Ω)	110.61W
Second Load (R=20Ω and L=30mH)	97.82W
Third Load (R=20Ω and L=39mH)	90.98W

3.2. Switching Losses

Since the utilized switches and diodes in power electronic converters are not ideal, they don't turn on and off instantly. This causes losses in the time of turning on and turning off the semiconductor devices. Therefore, the losses due to the once turning off is as follows.

$$E_{off} = \int_0^{t_{off}} V(t) i(t) dt = \int_0^{t_{off}} \left[\left(\frac{V_s}{t_{off}} t \right) \left(-\frac{I_s}{t_{off}} \left(t - t_{off} \right) \right) \right] dt = \frac{1}{6} V_s I_s t_{off} \quad (20)$$

In equation (20), $V(t)$ and $i(t)$ are the instance values of voltage and current of the switch during switching, respectively. Also, I_s and V_s is the switch's current before turning off and the switch's voltage after turning off, respectively. Also, t_{off} is the time when the switch is turned off. Similarly, the losses due to the once turning on is given as follows.

$$E_{on} = \int_0^{t_{on}} V(t) i(t) dt = \int_0^{t_{on}} \left[\left(\frac{V_s}{t_{on}} t \right) \left(-\frac{I_s}{t_{on}} \left(t - t_{on} \right) \right) \right] = \frac{1}{6} V_s I_s t_{on} \quad (21)$$

In equation (21), I_s and V_s is the current of the switch after turning on and the voltage of the switch before turning on. Also, t_{on} is the time when the switch is turned on. Moreover, the average switching losses (P_{sw}) are expressed as follows.

$$P_{sw} = 2f \left[\sum_{i=1}^{N_s} \left(\sum_{j=1}^{N_{on,i}} E_{on,ij} + \sum_{j=1}^{N_{off,i}} E_{off,ij} \right) \right] \quad (22)$$

In equation (22), $E_{off,ij}$, $E_{on,ij}$, $N_{off,i}$, and $N_{on,i}$ are the energy losses by the i_{th} switch when the switch is turned off for the j_{th} time, the energy losses by the i_{th} switch when the switch is turned on for the j_{th} time, the count of turning off of the i_{th} switch, and the count of turning on of the i_{th} switch, respectively. Also, N_s indicate the number of total switches [13].

The switching losses for various loads are provided in Table 4.

Table 4. The switching losses for various loads

Type of Load	Switching Losses
First Load (R=20Ω)	0.1W
Second Load (R=20Ω and L=30mH)	0.17W
Third Load (R=20Ω and L=39mH)	0.19W

3.2. Calculation of Efficiency

Considering P_c and P_{sw} according to Table 5, total losses (P_{loss}) and efficiency are obtained for three different loads.

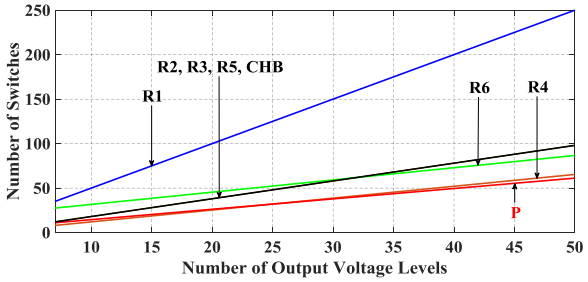
Table 5. The Losses and Efficiency for Three Various Loads

Load	P_{loss}	Efficiency
First Load	110.71W	95.08%
Second Load	97.99W	95.16%
Third Load	91.17W	95.23%

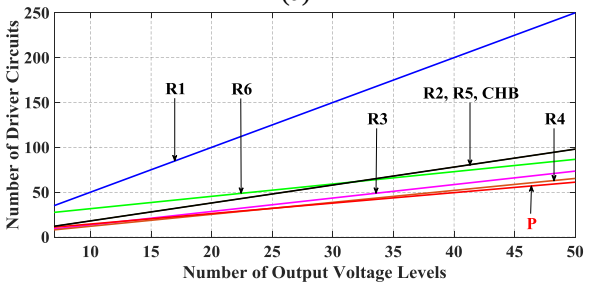
4. Comparative Study

In this part, to show the merits of the introduced inverter, the suggested circuit is compared in viewpoints of the N_s, N_{dr}, N_{DC}, and TSV for the same levels with some recent structures of MLIs. The comparison consists of two parts. In the first part, the proposed inverter is compared with the symmetric

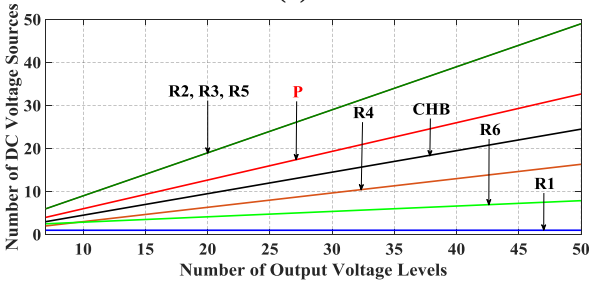
determination of input sources, with the symmetric CHB and the symmetric structures R1-R6, proposed in [5-8, 15, 16]. Also, in the second part, the proposed inverter with the asymmetric determination is compared with trinary CHB (3:1) and the asymmetric structures R7-R12, which are proposed in [9-12, 17, 18]. The comparison of the first part is demonstrated in Fig. 8. According to Fig. 8(a) and 8(b), the proposed structure is the best in the viewpoint of the count of switches and driver circuits. It should be noted that for both bidirectional and unidirectional switches, one driver circuit is considered. Moreover, Fig. 8(c) shows the superiority of the proposed structure over R2, R3, and R5 in terms of the N_{DC}. Besides, since in the proposed structure, the output of BM is connected to the H-bridge, so the TSV of the proposed structure is high. However, according to Fig. 8(d), the TSV of the proposed structure is less than R1 and R6. Also, in the second part, according to Fig. 9(a) and 9(b), the proposed structure is the best in terms of the number of switches and terms of the number of driver circuits, only weaker than R10 and R12. Furthermore, according to Fig. 9(c) and 9(d), the proposed circuit is only weaker than trinary CHB (3:1) and R10 in terms of the input sources, and in terms of the TSV, is better than R7-R9 and weaker than CHB (3:1) and R10-R12. However, the TSV of



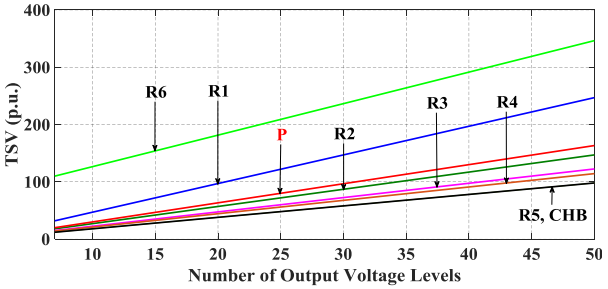
(a)



(b)

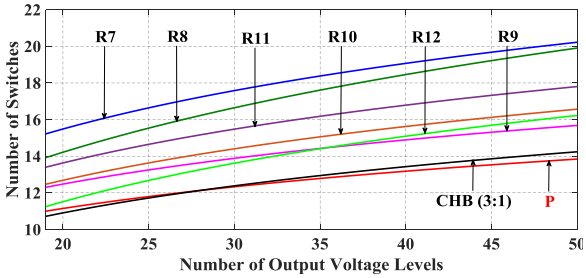


(c)

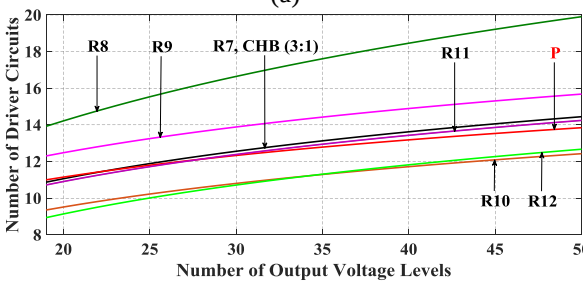


(d)

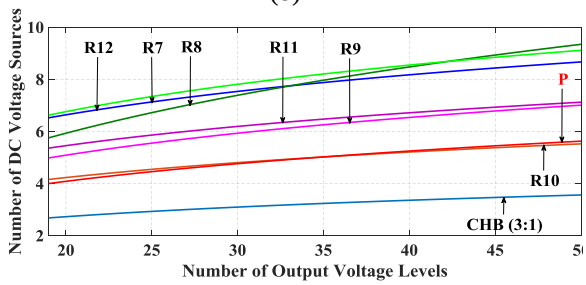
Figure 8. For symmetric topologies comparison of (a) N_s (b) N_{dr} (c) N_{DC} (d) TSV versus N_L



(a)

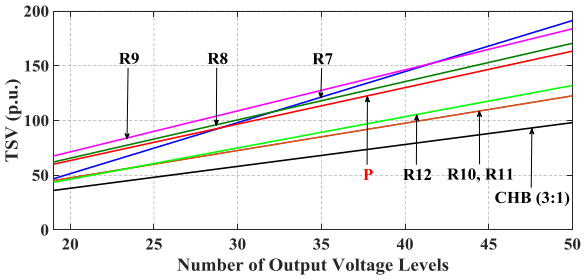


(b)



(c)

the proposed structure is acceptable and in the moderate range.



(d)

Figure 9. For asymmetric topologies comparison of (a) N_s (b) N_{dr} (c) N_{DC} (d) TSV versus N_L

5. Simulation Results

For simulations, implementations, and other studies, one circuit of the proposed structure is considered a case-study circuit. The case-study circuit consists of one BM and an H-bridge connected to it. According to Table 1, the case-study circuit with the first and second algorithms for determining the magnitude of input sources can generate seven and nineteen voltage levels, respectively. In this section, for demonstrating the performance and feasibility of the proposed inverter, the case-study circuit for both symmetric and asymmetric configurations is simulated in MATLAB/Simulink.

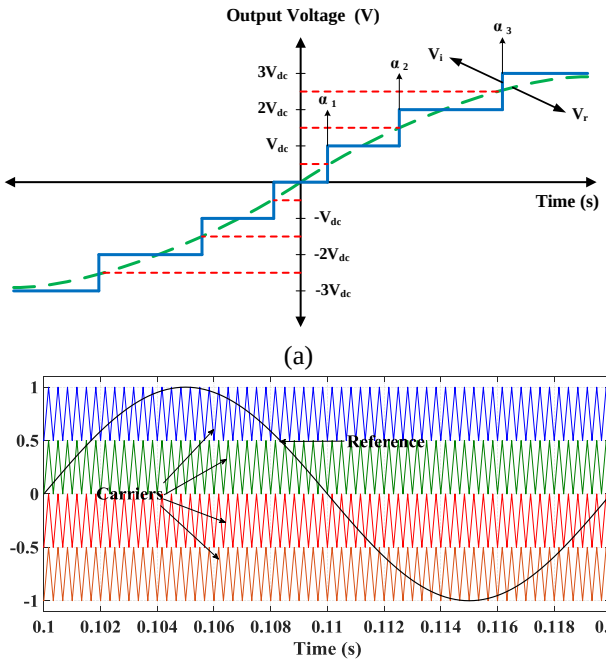
There are various modulation strategies for switching MLI switches. In this work, two strategies of LS-PWM and NLC, which are high and low frequency, respectively, have been used to switch the proposed structure due to the provision of appropriate power quality. In NLC, as shown in Fig. 10(a), the reference waveform is continuously sampled. So that if the sampled points are higher than the nearest DC offset, they are rounded to a higher voltage level and vice versa. Voltage levels in NLC change at certain angles, and because switching states change at these angles, they are also known as switching angles. The switching angle (α) in NLC is obtained as follows.

$$\alpha = \arcsin\left(\frac{i-0.5}{N_L}\right) \quad i = 1,\ldots,N_L \tag{23}$$

Another utilized switching strategy in this work is LS-PWM, in which, according to Fig. 10(b), a reference sine wave is compared to some carrier waves that are triangles, and the necessary gate commands for the inverter switches are provided. The number of required carrier waves to switch an MLI depends on the count of levels and is obtained from equation (24).

$$C = N_L - 1 \tag{24}$$

Whereas, C represents the number of utilized carrier waves in LS-PWM [19].



(a)

(b)

Figure 10. Diagram of modulation in (a) NLC (b) LS-PWM

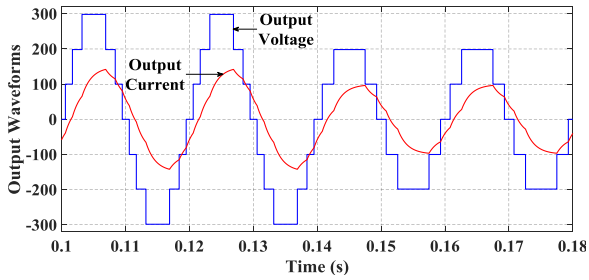
5.1. Simulation Results with NLC Strategy

Fig. 11(a) shows the simulation results of the voltage and current of a symmetrical structure for the second load (R=20Ω and L=30mH). Similarly, the output waveforms for the asymmetric structure are illustrated in Fig. 11(b). To demonstrate the inverter feasibility at different modulation indexes, the output voltage levels of symmetric and asymmetric configurations by reducing the modulation index from 1 to 0.7 in t=0.14s, are displayed in Fig. 11(a) and 11(b), respectively. It should be noted that in all simulation waveforms the output current is multiplied by ten.

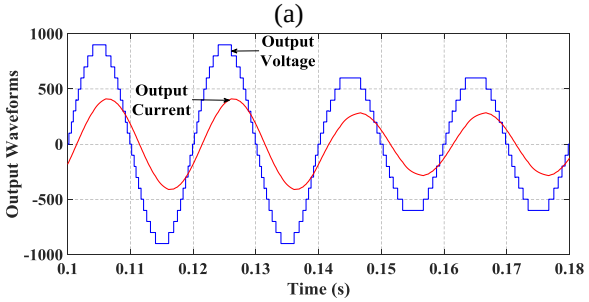
5.2. Simulation Results with LS-PWM Strategy

In this section, the output waveforms of symmetric and asymmetric configurations using LS-PWM for the second load (R=20Ω and L=30mH) are displayed in Fig. 12(a) and Fig. 12(b), respectively. Also, the output waveforms by using LS-PWM considering the change in modulation index from 1 to 0.7 in t=0.14s,

for symmetric and asymmetric configurations are given in Fig. 12(a) and Fig. 12(b), respectively. It should be noted that the frequency of LS-PWM is selected 3kHZ.

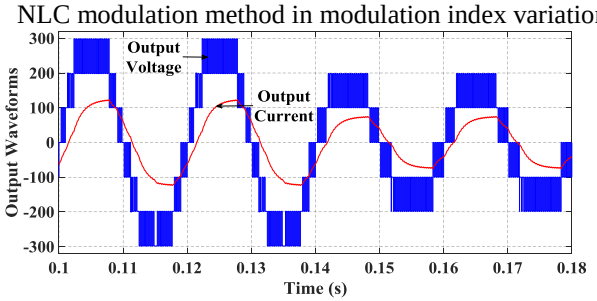


(a)

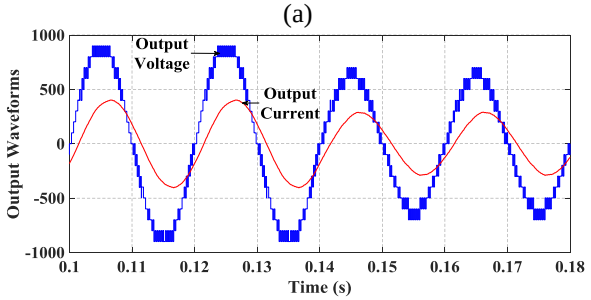


(b)

Figure 11. AC side of the introduced inverter using NLC modulation method in modulation index variation



(a)



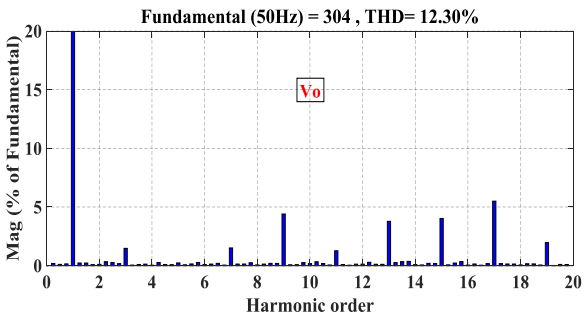
(b)

Figure 12. AC side of the introduced inverter using LS-PWM modulation method in modulation index variation from 1 to 0.7 for second load (a) symmetric (b) asymmetric

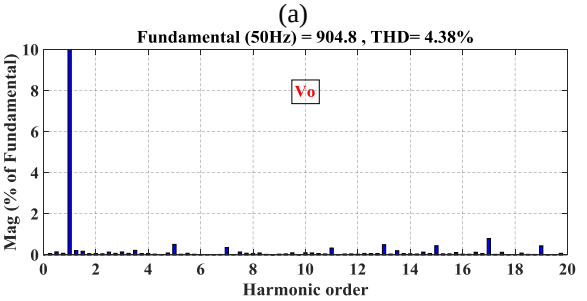
5.2. Comparative Study of Fast Fourier Transform (FFT) for NLC and LS-PWM

Fig. 13 illustrates the FFT of the voltage of symmetric and asymmetric configurations modulated by NLC. On the other hand, the FFT of the voltage of the introduced circuit for symmetric and asymmetric configurations using the LS-PWM method is demonstrated in Fig. 14.

By comparing the THD of the voltage in the two methods of NLC and LS-PWM, it is concluded that due to the high count of levels of the proposed structure, the THD of NLC is less than the LS-PWM, so NLC is more suitable for modulation of this structure.



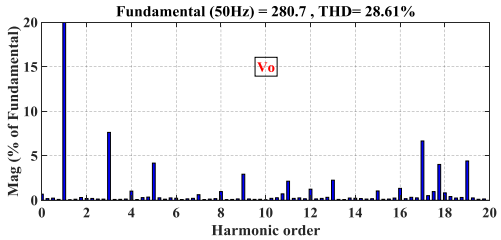
(a)



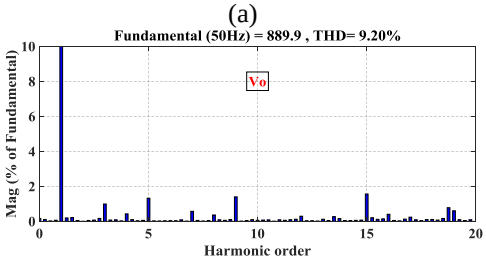
(b)

Figure 13. FFT of the voltage of the introduced inverter using NLC modulation method for (a) symmetric (b) asymmetric configurations

Moreover, simulation waveforms are used for applications in a photovoltaic system that feeds the inverter and the inverter feeds a linear induction motor. In this research, the P&O method is used to track the MPP, and each of the photovoltaic panels supplies one of the inverter voltage sources. In this case, the symmetric configuration of this inverter is used. The diagram of the simulation algorithm with PVs for Linear Induction Motor (LIM) is shown in Fig. 15. According to this figure, the proposed



(a)



(b)

Figure 14. FFT of the voltage of the introduced inverter using LS-PWM modulation method for (a) symmetric (b) asymmetric configurations

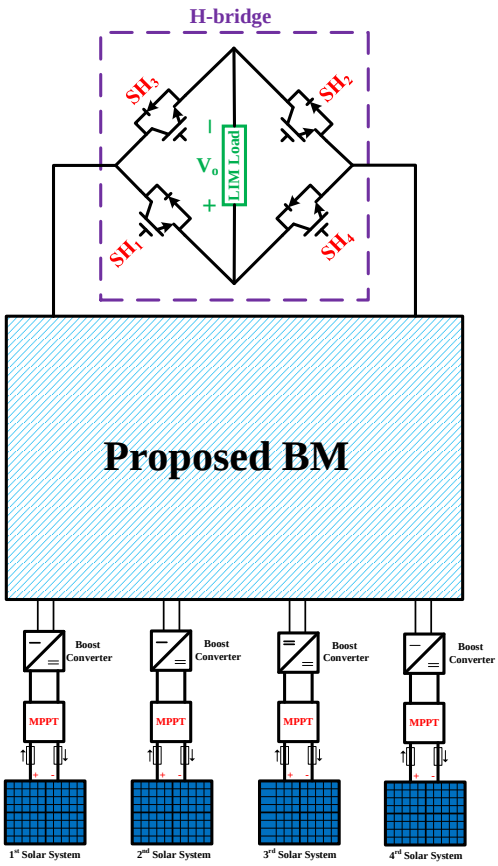


Figure 15. Simulation Diagram of the Proposed Inverter with PVs for LIM

inverter fed by PVs and the output of the inverter supplied the LIM.

Linear motors are motors that do not rotate unlike conventional motors, ie they do not have a rotor that rotates inside the stator or outside the stator, but the two parts of the motor move to each other. Therefore, the line goes back to the type of motor movement [20]. since have recently these motors been found in numerous applications, it has been used to demonstrate the proper operation of the inverter for an arbitrary application in which the inverter input is fed by PV and the output of the inverter supplies a linear induction motor.

Inverter output voltage is shown in Fig. 16. Furthermore, the waveforms of voltage, current, and power of the PV are shown in Fig. 17, Fig. 18, and Fig. 19, respectively.

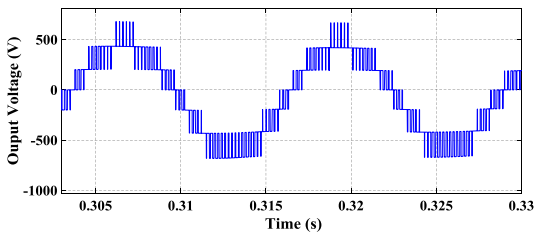


Figure 16. Output Voltage of the Inverter

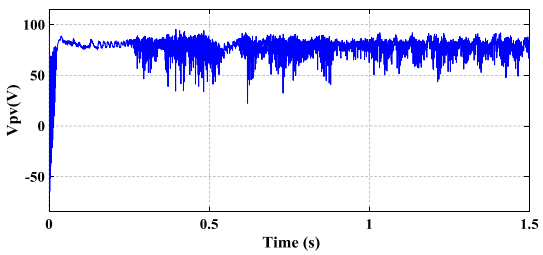


Figure 17. Output Voltage of the PV

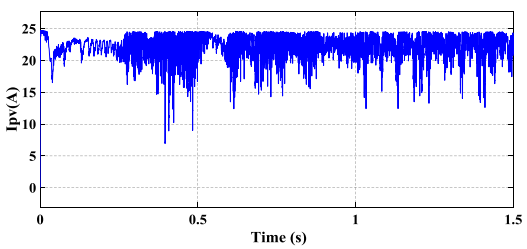


Figure 18. Output Current of the PV

The thrust force and speed for the used linear motor are shown in Fig. 20, and Fig. 21, respectively.

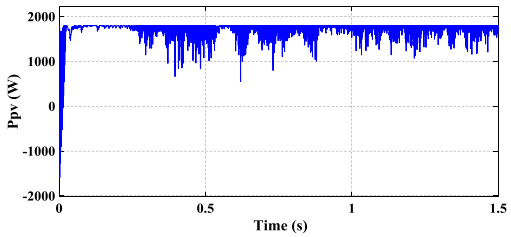


Figure 19. Output Power of the PV

According to these figures, it can be seen that the measured values of the linear motor trace the given reference values. It is observed that the thrust force increases in 0.5 and 0.9 seconds. For speed, the speed is increased and decreased in 0.5 and 0.9 seconds, respectively.

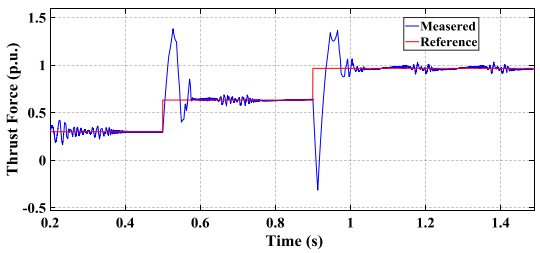


Figure 20. Thrust Force of the LIM

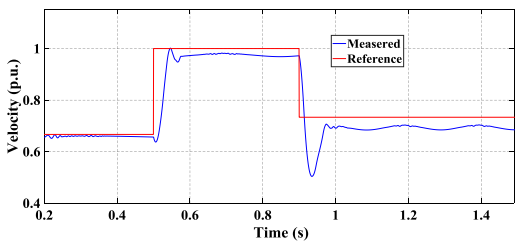


Figure 21. Velocity of the LIM

6. Experimental Results

Also, to validate the performance of the introduced structure in practice, the case-study circuit has been implemented for symmetric configurations using the NLC, and LS-PWM modulation methods by a DSP processor in a power electronics laboratory for the R=20Ω and L=30mH. Fig. 22 illustrates the output waveforms in both NLC and LS-PWM strategies.

7. Conclusion

In this research, a new structure for MLIs to decrease the count of power equipment was introduced. The new MLI circuit consisted of two parts, BM and H-bridge. So, that H-bridge was added

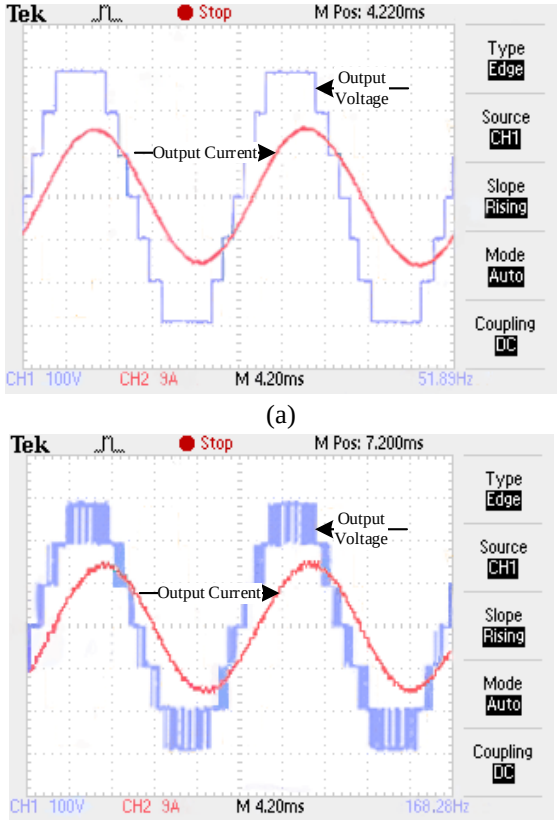


Figure 22. Experimental AC side of the symmetric configuration using (a) NLC (b) LS-PWM modulation method

due to the inability of BM to generate negative levels, and with the presence of the H-bridge, the MLI was able to produce all levels symmetrically. Also, the general circuit of the new MLI structure was illustrated. So that in this circuit, to increase the count of levels and thus reduce THD, more BMs easily were cascaded together. Moreover, the new structure of the MLI was studied with algorithms for determining the magnitude of input sources, and one circuit was selected as a case-study circuit. Also, the losses of the case-study circuit with symmetric configuration and NLC method were calculated for three various loads, which gave satisfactory results. Furthermore, the inverter performance provided for the linear induction motor-driven that the power was supported by PVs was demonstrated. Moreover, to show the merits and advantages of the introduced converter, the suggested structure was compared with CHB and some recent structures for MLIs in two sections of symmetric and asymmetric configurations. The comparison results showed a decrease in the count of utilized power equipment to produce the same voltage levels. Finally, to demonstrate the feasibility and

proper performance of the suggested inverter, the case-study circuit was simulated in the MATLAB/Simulink software with two modulation methods of NLC and LS-PWM, and its voltage FFT was shown in both asymmetric and symmetric configurations. In addition to the simulation results, the introduced circuit was implemented in the power electronics laboratory by a DSP processor, and the proper performance of the proposed inverter was proved.

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